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Engineering Note

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Subject: Charge signal distribution in MCM Test Board

The following table correlates which DAC channel drives which MCM and/or SVX Iie channel on the MCM Test Board. It also indicates the interface used for each connection and which SIFT within the MCM is exercised. The table columns are:

DAC #: Which channel of the DAC connection from the VTBG this is.
Qbus#: Which bit of the internal MCM Test Board Charge Bus this is.
MCM Channel: Which MCM channel, if any, is connected to this signal.
Which SIFT: Which SIFT of the four in the MCM, if any, is connected to this signal.
SVX Channel: Which SVX Iie channel, if any, is connected to this signal.
Function: Shorthand description of interface circuit between DAC output and charge input.

After using up all 64 DAC channels many inputs of the MCM and SVX Iie are left over. These are connected to various test schemes:

CONN indicates that the input is brought out to a header which allows connection of external signals.

AGND indicates that the input is grounded.

TREF indicates that the input is connected to one channel of an internal pulser which is time-synchronized with other charge data.

CREF indicates that these inputs are all tied together to a common reference pulse which is also time-synchronized with other charge data.

The timing relationship between the TREF pulse, the CREF pulse and other charge data is variable by programming the board. Two channels of the DAC are connected to comparators and do not drive any charge sensitive inputs. The comparator outputs are presented to the digital logic to provide extra timing information and/or scope triggers.

DAC #	Qbus #	MCM Channel	Which SIFT	SVX Channel	Function
0	0	2	1	N/C	Discrete component, parallel term, Q split between MCM &
1	1	10	1	N/C	Discrete component, parallel term, Q split between MCM &
2	2	17	1	N/C	Discrete component, parallel term, Q split between MCM &

3	3	23	1	N/C	Discrete component, parallel term, Q split between MCM &
4	4	32	2	N/C	Discrete component, parallel term, Q split between MCM &
5	5	41	2	N/C	Discrete component, parallel term, Q split between MCM &
6	6	48	2	N/C	Discrete component, parallel term, Q split between MCM &
7	7	56	2	N/C	Discrete component, parallel term, Q split between MCM &
8	8	62	2	N/C	Discrete component, parallel term, Q split between MCM &
9	9	72	3	N/C	Discrete component, parallel term, Q split between MCM &
10	10	78	3	N/C	Discrete component, parallel term, Q split between MCM &
11	11	87	3	N/C	Discrete component, parallel term, Q split between MCM &
12	12	94	3	N/C	Discrete component, parallel term, Q split between MCM &
13	13	103	4	N/C	Discrete component, parallel term, Q split between MCM &
14	14	109	4	N/C	Discrete component, parallel term, Q split between MCM &
15	15	118	4	N/C	Discrete component, parallel term, Q split between MCM &
16	16	6	1	N/C	Network component, parallel term, Q split between MCM &
17	17	13	1	N/C	Network component, parallel term, Q split between MCM &
18	18	21	1	N/C	Network component, parallel term, Q split between MCM &
19	19	28	1	N/C	Network component, parallel term, Q split between MCM &
20	20	37	2	N/C	Network component, parallel term, Q split between MCM &
21	21	43	2	N/C	Network component, parallel term, Q split between MCM &
22	22	52	2	N/C	Network component, parallel term, Q split between MCM &
23	23	59	2	N/C	Network component, parallel term, Q split between MCM &
24	24	68	3	N/C	Network component, parallel term, Q split between MCM &
25	25	74	3	N/C	Network component, parallel term, Q split between MCM &
26	26	82	3	N/C	Network component, parallel term, Q split between MCM &
27	27	91	3	N/C	Network component, parallel term, Q split between MCM &
28	28	98	4	N/C	Network component, parallel term, Q split between MCM &
29	29	107	4	N/C	Network component, parallel term, Q split between MCM &
30	30	112	4	N/C	Network component, parallel term, Q split between MCM &
31	31	123	4	N/C	Network component, parallel term, Q split between MCM &
32	32	N/C	N/A	0	Network component, parallel term, Q split between SVX &
33	33	N/C	N/A	11	Network component, parallel term, Q split between SVX &
34	34	N/C	N/A	21	Network component, parallel term, Q split between SVX &
35	35	N/C	N/A	31	Network component, parallel term, Q split between SVX &
36	36	N/C	N/A	41	Discrete component, parallel term, Q split between SVX &
37	37	N/C	N/A	51	Discrete component, parallel term, Q split between SVX &
38	38	N/C	N/A	61	Discrete component, parallel term, Q split between SVX &
39	39	N/C	N/A	71	Discrete component, parallel term, Q split between SVX &

40	40	7	1	N/C	Discrete component, serial term, Q split between MCM & A
41	41	46	2	N/C	Discrete component, serial term, Q split between MCM & A
42	42	77	3	N/C	Discrete component, serial term, Q split between MCM & A
43	43	110	4	N/C	Discrete component, serial term, Q split between MCM & A
44	44	N/C	N/A	81	Discrete component, serial term, Q split between SVX & A
45	45	N/C	N/A	91	Discrete component, serial term, Q split between SVX & A
46	46	N/C	N/A	101	Discrete component, serial term, Q split between SVX & A
47	47	N/C	N/A	111	Discrete component, serial term, Q split between SVX & A
48	48	26	1	N/C	1 st part of 4-way charge split
48	49	27	1	N/C	2 nd part of 4-way charge split
48	50	N/C	N/A	5	3 rd part of 4-way charge split
48	51	N/C	N/A	15	4 th part of 4-way charge split
49	52	83	3	N/C	1 st part of 4-way charge split
49	53	84	3	N/C	2 nd part of 4-way charge split
49	54	N/C	N/A	25	3 rd part of 4-way charge split
49	55	N/C	N/A	35	4 th part of 4-way charge split
50	56	42	2	N/C	Optocoupled (photodiode) charge pulse.
51	57	71	3	N/C	Optocoupled (photodiode) charge pulse.
52	58	117	4	N/C	Optocoupled (photodiode) charge pulse.
53	59	N/C	N/A	45	Optocoupled (photodiode) charge pulse.
54	60	11	1	N/C	1 st part of 2:1 even charge split (half to MCM, half to SVX)
54	61	N/C	N/A	55	2 nd part of 2:1 even charge split (half to MCM, half to SVX)
55	62	22	1	N/C	1 st part of 2:1 even charge split (half to MCM, half to SVX)
55	63	N/C	N/A	65	2 nd part of 2:1 even charge split (half to MCM, half to SVX)
56	64	47	2	N/C	1 st part of 2:1 even charge split (half to MCM, half to SVX)
56	65	N/C	N/A	75	2 nd part of 2:1 even charge split (half to MCM, half to SVX)
57	66	57	2	N/C	1 st part of 2:1 even charge split (half to MCM, half to SVX)
57	67	N/C	N/A	85	2 nd part of 2:1 even charge split (half to MCM, half to SVX)
58	68	73	3	N/C	1 st part of 2:1 even charge split (half to MCM, half to SVX)
58	69	N/C	N/A	95	2 nd part of 2:1 even charge split (half to MCM, half to SVX)
59	70	88	3	N/C	1 st part of 2:1 even charge split (half to MCM, half to SVX)
59	71	N/C	N/A	105	2 nd part of 2:1 even charge split (half to MCM, half to SVX)
60	72	99	4	N/C	1 st part of 2:1 even charge split (half to MCM, half to SVX)
60	73	N/C	N/A	115	2 nd part of 2:1 even charge split (half to MCM, half to SVX)
61	74	119	4	N/C	1 st part of 2:1 even charge split (half to MCM, half to SVX)
61	75	N/C	N/A	124	2 nd part of 2:1 even charge split (half to MCM, half to SVX)
62	76	N/C	N/A	N/C	Connected to voltage comparator for digital timing reference

63	77	N/C	N/A	N/C	Connected to voltage comparator for digital timing reference.
AGND	AGND	5	1	N/C	Channel input tied to board analog ground for reference.
AGND	AGND	12	1	N/C	Channel input tied to board analog ground for reference.
AGND	AGND	29	1	N/C	Channel input tied to board analog ground for reference.
AGND	AGND	38	2	N/C	Channel input tied to board analog ground for reference.
AGND	AGND	49	2	N/C	Channel input tied to board analog ground for reference.
AGND	AGND	58	2	N/C	Channel input tied to board analog ground for reference.
AGND	AGND	67	3	N/C	Channel input tied to board analog ground for reference.
AGND	AGND	81	3	N/C	Channel input tied to board analog ground for reference.
AGND	AGND	92	3	N/C	Channel input tied to board analog ground for reference.
AGND	AGND	102	4	N/C	Channel input tied to board analog ground for reference.
AGND	AGND	108	4	N/C	Channel input tied to board analog ground for reference.
AGND	AGND	120	4	N/C	Channel input tied to board analog ground for reference.
AGND	AGND	N/C	N/A	2	Channel input tied to board analog ground for reference.
AGND	AGND	N/C	N/A	13	Channel input tied to board analog ground for reference.
AGND	AGND	N/C	N/A	23	Channel input tied to board analog ground for reference.
AGND	AGND	N/C	N/A	33	Channel input tied to board analog ground for reference.
AGND	AGND	N/C	N/A	43	Channel input tied to board analog ground for reference.
AGND	AGND	N/C	N/A	53	Channel input tied to board analog ground for reference.
AGND	AGND	N/C	N/A	63	Channel input tied to board analog ground for reference.
AGND	AGND	N/C	N/A	73	Channel input tied to board analog ground for reference.
AGND	AGND	N/C	N/A	83	Channel input tied to board analog ground for reference.
AGND	AGND	N/C	N/A	93	Channel input tied to board analog ground for reference.
AGND	AGND	N/C	N/A	103	Channel input tied to board analog ground for reference.
AGND	AGND	N/C	N/A	113	Channel input tied to board analog ground for reference.
AGND	AGND	N/C	N/A	123	Channel input tied to board analog ground for reference.
CONN	CONN	97	4	N/C	Connected to header for user input.
CONN	CONN	104	4	N/C	Connected to header for user input.
CONN	CONN	N/C	N/A	7	Connected to header for user input.
CONN	CONN	N/C	N/A	9	Connected to header for user input.
CONN	CONN	N/C	N/A	17	Connected to header for user input.
CONN	CONN	N/C	N/A	19	Connected to header for user input.
CONN	CONN	N/C	N/A	27	Connected to header for user input.
CONN	CONN	N/C	N/A	29	Connected to header for user input.
CONN	CONN	N/C	N/A	37	Connected to header for user input.
CONN	CONN	N/C	N/A	39	Connected to header for user input.
CONN	CONN	N/C	N/A	47	Connected to header for user input.

CONN	CONN	N/C	N/A	49	Connected to header for user input.
CONN	CONN	N/C	N/A	57	Connected to header for user input.
CONN	CONN	N/C	N/A	59	Connected to header for user input.
CONN	CONN	N/C	N/A	67	Connected to header for user input.
CONN	CONN	N/C	N/A	69	Connected to header for user input.
CONN	CONN	N/C	N/A	77	Connected to header for user input.
CONN	CONN	N/C	N/A	79	Connected to header for user input.
CONN	CONN	N/C	N/A	87	Connected to header for user input.
CONN	CONN	N/C	N/A	89	Connected to header for user input.
CONN	CONN	N/C	N/A	97	Connected to header for user input.
CONN	CONN	N/C	N/A	99	Connected to header for user input.
CONN	CONN	N/C	N/A	107	Connected to header for user input.
CONN	CONN	N/C	N/A	109	Connected to header for user input.
CONN	CONN	N/C	N/A	117	Connected to header for user input.
CONN	CONN	N/C	N/A	119	Connected to header for user input.
CONN	CONN	N/C	N/A	121	Connected to header for user input.
TREF	TREF	16	1	N/C	Time-synchronized charge pulse from CLKGEN; split to ea
TREF	TREF	36	2	N/C	Time-synchronized charge pulse from CLKGEN; split to ea
TREF	TREF	66	3	N/C	Time-synchronized charge pulse from CLKGEN; split to ea
TREF	TREF	111	4	N/C	Time-synchronized charge pulse from CLKGEN; split to ea
CREF	CREF	20	1	N/C	Time-synchronized charge pulse from CLKGEN; channels t together
CREF	CREF	53	2	N/C	Time-synchronized charge pulse from CLKGEN; channels t together
CREF	CREF	124	4	N/C	Time-synchronized charge pulse from CLKGEN; channels t together